Toward High-Performance Digital Logic Technology with Carbon Nanotubes

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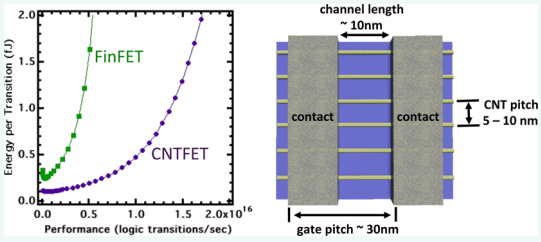
ABSTRACT The slow-down in traditional silicon complementary metal-oxide–semiconductor (CMOS) scaling (Moore's law) has created an opportunity for a disruptive innovation to bring the semiconductor industry into a postsilicon era. Due to their ultrathin body and ballistic transport, carbon nanotubes (CNTs) have the intrinsic transport and scaling properties to usher in this new era. The remaining challenges are largely materials-related and include obtaining purity levels suitable for logic technology, placement of CNTs at very tight (~5 nm) pitch to allow for density scaling and source/drain contact scaling. This review examines the potential performance advantages of a CNT-based computing technology, outlines the remaining challenges, and describes the recent progress on these fronts. Although overcoming these issues will be challenging and will require a large, sustained effort from both industry and academia, the recent progress in the field is a cause for optimism that these materials can have an impact on future technologies.



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The foundation for the unprecedented success of the microelectronics industry was laid in 1965 with the observation of Moore's law, projecting the doubling of components on a chip every 18 months, along with the formulation of the metal-oxide–semiconductor field-effect-transistor (MOSFET) scaling laws outlined by Dennard in 1974.[1] Moore's law provided the business incentive for increasing productivity, while Dennard's law provided the recipe for increasing component density. The semiconductor industry progressed following these rules for over three decades, until the early 2000s when major materials changes (as opposed to changing the scaling dimensions) started to be necessary at nearly every technology node to maintain control of the electron flow in the shrinking transistor channel.[2] These changes include silicon lattice straining, high-κ gate stack materials, and trigate device geometry. Such innovations required dramatic engineering efforts and have slowed device scaling, intensifying the search for the "next switch" with the goal of finding a new switching element that can replace the conventional Si transistor.[2,3]

Transistor technology must maintain a crucial balance between power, performance, and density. Power constraints have limited the performance gains in silicon complementary metal-oxide–semiconductor (CMOS) technology for nearly 10 years, as measured by the clock frequency. This performance stall is largely attributed to an inability to scale the operating voltage of Si MOSFETs below approximately 1 V. Despite the power constraints, the economics of Moore's law will continue to drive density scaling, which will ultimately necessitate a drop in device performance. The development of a next switch that can deliver performance improvements when scaled, along with the ability to operate at voltages <0.5 V to reduce power consumption, has led to the consideration of new materials for the transistor channel.

Single-walled carbon nanotubes (CNTs) were initially hailed as a potential next switch in the early 2000s, but interest in CNT-based devices waned due to difficulties associated with the purification and controlled placement of semiconducting CNTs. In this review, we revisit the application of CNT-based

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devices for high-density logic circuits, discuss recent progress on the remaining problems, and outline a path for how CNTs could be a solution for the 7−5 nm technology nodes. The review is sectioned as follows:

(a) Motivate the study by showing the potential performance advantages of CNT logic *versus* scaled silicon digital technology
(b) Illustrate what the CNTFET device geometry will need to "look" like at the 5 nm technology node based on the system-level modeling
(c) Materials challenges and methods for sorting CNTs
(d) Requirements and methods for placement of CNTs
(e) Device related challenges

Traditional Scaling Path. The primary challenges to scaling transistors for the coming technology generations are related to the gate losing control over the current in the channel. Continued decreasing of the gate dielectric thickness, even through using higher dielectric constant insulators, increases gate electrostatic control, but also increases gate leakage current that adversely contributes to the static power. Under Dennard scaling,[1] the electric field in a device was kept constant so that reduction in lengths would be appropriately accommodated for by increased channel doping, decreased junction depth, thinner gate dielectrics and decreased voltages. Physical limits to material thicknesses and control of the placement of dopants are major barriers to increasing performance.

Currently, there is no demonstrated solution to push conventional bulk silicon (doping-controlled) devices below the 20 nm gate length mark.[3] To push gate length scaling further, the industry is moving toward thin-body devices such as FinFETs (where the silicon is patterned to form a thin, fin-like structure with the gate covering the channel on three sides), also known as 3D or trigate FETs.[2] The performance parameters of these thin-body devices are controlled solely by the transistor body or channel thickness such that the body thickness will determine the minimum gate length (L_{min}) at which the current can be effectively modulated by the gate. In the case of a FinFET, $L_{min} \sim 2\ D_{fin}$ (where D_{fin} is defined as the thickness of the Fin structure) due to the 3D multigated device structure. To push gate lengths below 10 nm, Fin widths of <5 nm are necessary. Reducing the channel width to such dimensions would likely result in a dramatic mobility loss and unacceptable threshold variation due to Fin width tolerances in the manufacturing process. In the more extreme case, the FinFET is converted to a nanowire with a gate-all-around geometry giving an improved scaling behavior where L_{min} can be $\sim 1.2-1.5 \times d_{wire}$ allowing for shorter channel lengths at the same body thickness as compared to FinFETs. For the 5 nm technology node, a gate length of 8 nm is required, which would necessitate a wire diameter between 5 and 7 nm. While Si devices and circuits have been demonstrated in this diameter range, it is not clear that they can deliver the needed performance at the desired integration densities.

There is increasing focus on high mobility channel materials (such as Ge for p-type FETs (PFETs) and III/V materials for n-type FETs (NFETs)) for their potential to improve device performance and enable lower operating voltages. Despite their high mobility, adverse quantum confinement effects in III/V materials are expected to dominate at longer channel lengths than in Si or Ge due to the small carrier effective masses in these materials. The light carrier effective mass will also make III/V material channels more sensitive to direct source-drain tunneling, limiting gate length scaling. Additionally, there are severe challenges to integrating III−V devices, including the scaling of series resistance, engineering the dielectric/channel interface, and junction formation, all of which have been subjects of intensive research for decades.

Carbon Nanotubes. As continued scaling requires reduction of the channel thickness to maintain gate control, it is natural to consider using pure one- or two-dimensional materials so as to decouple vertical and lateral scaling (due to their extremely thin bodies), which will offer a path for further electrostatic improvement. Due to its lack of a bandgap, it is now clear that graphene is not suited for high-density integrated logic circuits. While techniques for opening a bandgap in graphene were shown, they all come at the cost of performance (increasing scattering or high voltages, *etc.*).[4−7] CNTs provide the superior transport properties of graphene with the addition of an intrinsic bandgap, making them an ideal candidate for the channel in a scaled transistor. A tangible demonstration of their potential is the recent fabrication of a functional CNT computer.[8]

Since their discovery, carbon nanotubes have drawn considerable attention due to their outstanding electrical, thermal and mechanical properties.[9−15] In particular, their transport properties benefit from superior electrostatics, due to an ultrathin body (1 atomic layer thick shell wrapped in a ~1 nm diameter cylinder), and ballistic transport at relatively long channel lengths.[9,16] In fact, the superior electrostatics were experimentally verified *via* the fabrication of sub-10 nm gate length transistors (Figure 1a−c) that show superior transport properties to that of silicon devices, while operating at substantially lower voltages.[10] The superior electrical properties at lower operating voltage will, in principal, translate to improved energy efficiency as the individual devices are integrated at a system level. Although such systems cannot currently be fabricated, system-level modeling using an optimizer program provides insight into the potential performance for the technology. Typically, the primary objective is to

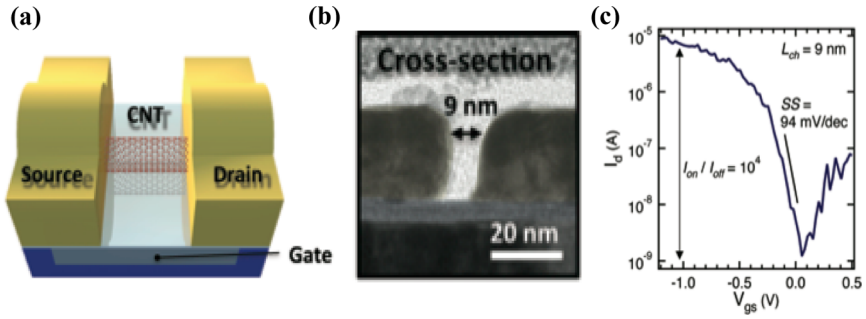


Figure 1. Scaled carbon nanotube transistor. (a) Schematic of CNTFET with a local bottom gate and (b) corresponding cross-sectional SEM image of a 9 nm device with a (c) representative IV curve of the device showing excellent switching behavior. Reproduced with permission from ref 10. Copyright 2012 American Chemical Society.

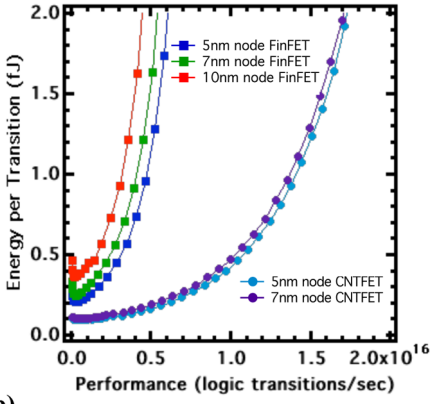
obtain as much performance as possible at a fixed power consumption.

To investigate this optimization problem for new classes of devices, we use a system optimization program, loosely based on IBM's Power 7 microprocessor, to capture the basic elements for determining chip performance.[17] The program solves a multidimensional optimization problem where various technological parameters are optimized to converge on a desired performance goal. In a typical case, certain parameters (*e.g.*, wire pitch, gate pitch) remain fixed, while others (*e.g.*, gate length, dielectric thickness, doping levels, body thickness) are optimized. In principal, this process identifies the key technological parameters for obtaining the highest processor performance at a given power budget. The program was verified for accuracy by reproducing well-known parameters for several *existing* technologies. This verification gives us confidence that this approach can predict the performance of future technologies given accurate device level input.

Figure 2a is a plot of performance (logic transitions per second) *versus* energy per transition for FinFET technology from the 10 to the 5 nm node and for CNTFET technology for the 7 and 5 nm node. The 7 and 5 nm node technologies were chosen because they represent both when the performance benefits stall in FinFETs (due to continued thinning of the body) and a realistic time frame for when a CNTFET technology could be ready assuming sufficient progress (~2020). In all cases, the wiring pitch and minimum gate pitch are fixed as they are completely dictated by the density scaling of the technology node (transistor density on a chip). In the case of the CNTFET technology, the gate length, CNT pitch, and CNT number per device were also found by the optimizer. The CNTFETs were in the gate-all around geometry, which was experimentally shown.[18]

As evidenced in Figure 2a, the optimizer program predicts a greater than two-fold improvement in the performance along with a greater than two-fold decrease in energy for the CNTFET as compared to FinFET technology, yielding nearly a five-fold improvement in the energy-delay product. The reason for the performance improvement is based on the superior transport properties of the CNTs that allow for a reduction of the

(a)



(b)

Parameters	CNT Processor
Gate Pitch	30 nm
Inter-CNT Pitch	8 nm
CNT Diameter	1.7 nm
# CNT/Transistor	6
Gate Length	11.3 nm
On-Current	5.93 uA/CNT
Off-Current	16.9 nA/CNT
I_{ON}/I_{OFF}	349
Sub-Threshold Swing	83.2 mV/decade
On-State Resistance	20.5 kOhm/CNT
High-K Thickness	2 nm

Figure 2. Modeling data for a CNT based logic technology. (a) Energy *versus* performance for both FinFET and CNTFET technologies. The data reveals a greater than two-fold improvement in both performance and energy per transition when going from Si FinFET to CNTFET technology. (b) Table of the CNT parameters determined by the optimizer program (at V_{dd} ~ 0.3 V).

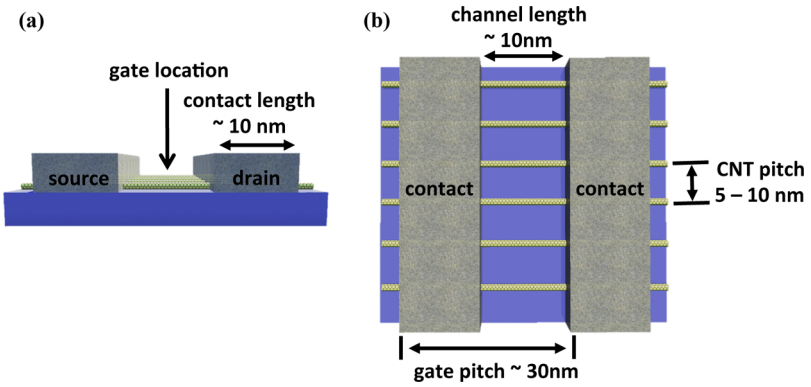


Figure 3. Schematic of a CNTFET modeled for the 5 nm technology node. (a) Side view of the device showing the CNT spanning the source and drain. The gate would be built either around each CNT or on top of the array and was removed for clarity. (c) Top view of the device showing multiple CNTs spanning the contacts. The key dimensions are the gate pitch and CNT pitch.

supply voltage (to around 50% of the supply voltage of the FinFET case), while maintaining performance. The optimized device parameters are shown in Figure 2b. This particular optimization was for a high-performance system (representing just one point on the curve near the elbow in Figure 2a), thus pushing for higher performance at the expense of low power operation yielding a modest I_{on}/I_{off}. The performance parameters are optimized for every point on the curve and vary with the desired power/performance trade-off. It is encouraging that the device-level performance targets (*i.e.*, *on*- and *off*-current, subthreshold swing, and *on*-state resistance) are values routinely demonstrated in scaled CNTFETs. Although the optimizer gives specific values for CNT diameter, CNTs/device, CNT pitch and gate length; these values can ultimately vary as long as the gate pitch and performance is preserved.

A schematic of such a device is illustrated in Figure 3. In short, achieving a viable CNT logic technology is, in effect, developing the processes needed to fabricate this device with high yield. The materials and fabrication requirements, listed below, will be discussed in the following sections.

1. Semiconducting purity of ppb
2. Placing CNTs with a well-defined and small pitch (<5−10 nm)
3. A CNT gate length and *contact length* of ∼8−12 nm

CNT Material Requirements. The materials requirements are derived directly from the device characteristics and geometry. The three parameters that will be discussed here include (1) the semiconducting *versus* metallic purity (determined by the number of CNTs on the chip), (2) the upper and lower limits of the CNT diameter (constrained by source-drain tunneling and *on*-state resistance, respectively) and the (3) diameter distribution (determined by threshold voltage (V_t) variation). All of these parameters are interrelated and greatly contribute to the device performance and device-to-device variability.

Any CNTFETs that contain one or more metallic CNTs cannot turn off and will result in a shorted device. If CNTs are to be a drop-in replacement for silicon CMOS devices, where there are no shorted devices, the purity requirements are simple (all metallic CNTs must be eliminated). Since the 5 nm technology node will have ∼10 billion transistors and each transistor will have ∼6 CNTs, along with expectations of a high manufacturing yield, the metallic CNT content must be <0.01 ppb. There are methods described in the literature that allow for some redundancy in devices that could tolerate a small number of shorted transistors,[8,19] but this compromises critical space on a chip where device density is of great importance. Even if such redundancies are built into the circuit design, the purity constraint would still require extremely high purity levels of ∼0.1−1 ppb.

CNTs vary in diameter from, typically, 0.6 to 2 nm. The diameter obtained is usually determined by the growth process where metal particle catalyzed syntheses (*i.e.*, HipCo or CoMoCat) typically grow CNTs with smaller diameters (<1 nm) and synthesis *via* laser ablation or arc discharge yields CNTs with larger diameters (>1 nm). For this review, the only factor we consider in defining diameter ranges is the effect diameter has on the device properties. As the diameter is inversely proportional to the bandgap, coupled with CNTFETs behaving as Schottky barrier-controlled devices, the diameter effect is rather straightforward. As the diameter of the CNT shrinks, thus increasing the bandgap, the contacts behave less Ohmic and introduce increasing levels of contact resistance. This was experimentally shown in Chen *et al.*[20] The results show that ideal Ohmic contacts are realized for CNTs with a diameter greater than 1 nm. The upper limit is a bit more difficult to define. As the diameter increases, and the bandgap shrinks, there is an increase in the *off*-state leakage current in a device. The optimizer program tends to favor diameters in the 1.7 nm range to push for higher drive currents, but with higher *off*-state current. The higher *off*-state current can be tolerated due to the significantly reduced supply voltage. On the basis of our

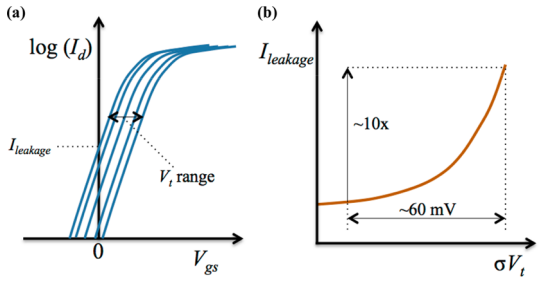


Figure 4. Illustration of the impact of threshold voltage variation on leakage current. (a) Plot showing how $I_{leakage}$ is affected by the V_t of a device and further how devices with a small range of V_t can have a large range of $I_{leakage}$. (b) Plot illustrating the impact of a variation in V_t on $I_{leakage}$, indicating the importance of a tight distribution in V_t.

present understanding, the likely CNT diameter range would be greater than ~1.2 nm, up to the diameter where source-drain tunneling is too severe, likely 1.7−2 nm.

The variation in diameter directly impacts the variation in threshold voltage. When integrated at a high density, it becomes crucial for the threshold voltage (V_t) of transistors to be as uniform as possible. A small V_t range is also desirable to control the passive power on a chip. The passive power is the power that is dissipated when transistors are in the *off*-state and is predominantly related to the leakage or *off*-current ($I_{leakage}$ or I_{off}), which is the current in a device at zero gate bias (Vgs). An illustration of how different V_t affects leakage is given in Figure 4, showing how a small range in V_t can have a dramatic impact on $I_{leakage}$. For a transistor with an ideal subthreshold swing (SS), a difference in V_t of 60 mV will yield a shift in $I_{leakage}$ of approximately an order of magnitude.

For CNTFETs, the diameter of the CNT will affect the resulting V_t. Because carrier injection from the source to the CNT takes place at a metal−semiconductor Schottky junction, the Schottky barrier height (SBH) governs the voltage needed to switch the device to the *on*-state. A change in d_{CNT} will cause an inversely proportional change in the bandgap (E_g), thus modifying the SBH. Assuming the CNT work function to be the same for all d_{CNT}, the V_t would change by approximately 50% of the E_g variation. The relationship between d_{CNT} and V_t has been modeled,[21] showing that variation at small diameters (<1 nm) results in greater than 1:1 ratio impact on V_t, while variation at larger diameters (>1.4 nm) results in a lessened impact on V_t. An additional consideration is how many CNT channels there will be in each CNTFET. Interestingly, if SS is the same for each CNT in the channel then I_{off} will be set by the CNT with the largest d_{CNT} (smallest E_g), which further illustrates why the V_{th} distribution must be as tight as possible.

Methods for Sorting Carbon Nanotubes. Ideally, one would like to grow the exact type of CNT needed: all semiconducting, of a specific diameter or with a narrow

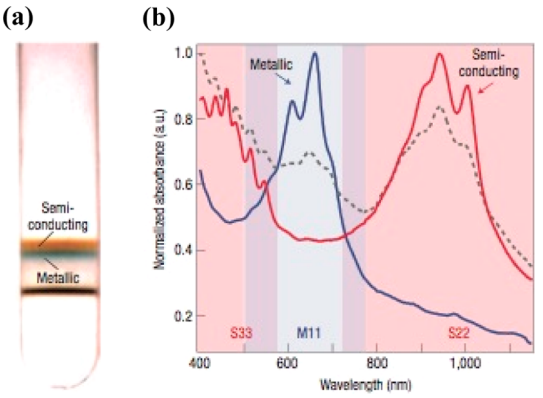


Figure 5. Sorting of carbon nanotubes by density gradient ultracentrifugation (DGU). (a) Optical image of CNTs sorted by electronic type using DGU. (b) UV−vis-NIR absorption spectra of sorted CNTs showing complete attenuation of the metallic region (M11) in the semiconducting (red curve) sample. Reproduced with permission from ref 23. Copyright Nature Publishing group 2006.

diameter range on a substrate at the required pitch (~5 nm). So far, such precise growth has not been demonstrated. Therefore, most integration schemes rely on postgrowth processing to sort the CNTs by electronic type and diameter. The following section will review the methods that are most promising for realizing the materials requirements. It does not cover all the separation methods in the literature,[22] but several of the most promising routes for producing CNTs that are suitable for high performance computing will be reviewed here.

Density gradient ultracentrifugation (DGU) is a technique that can be used to sort carbon nanotubes suspended in an aqueous surfactant mixture by their electronic type,[23] diameter[24] and even handedness.[25] The CNTs are first suspended in a surfactant mixture, then loaded into a centrifuge tube that contains a linear density gradient. After centrifugation, the CNTs will migrate to a point where their buoyant density matches that of the surrounding fluid at a point in the density gradient (see Figure 5). By carefully choosing the type of surfactant(s) and tuning the process conditions, one can resolve the CNTs by electronic type. A semiconducting purity of >99% has been achieved using DGU, which is at the detection limit of the optical techniques used to measure the purity; thus, the purity could very well be higher (section 3.5 contains a discussion on metrology restraints). In addition to optical spectroscopy, fabrication and testing of electrical devices also show a high-degree of semiconducting enrichment.[26−29] This route is particularly promising as it is scalable (see nanointegris.com), has already produced highly purified materials, is effective in a variety of diameter ranges and may allow for the purity levels necessary for high-performance computing.

An alternative method to sorting CNTs is column chromatography,[30−34] which proceeds in a fashion similar to DGU. In this method, the CNTs are first suspended

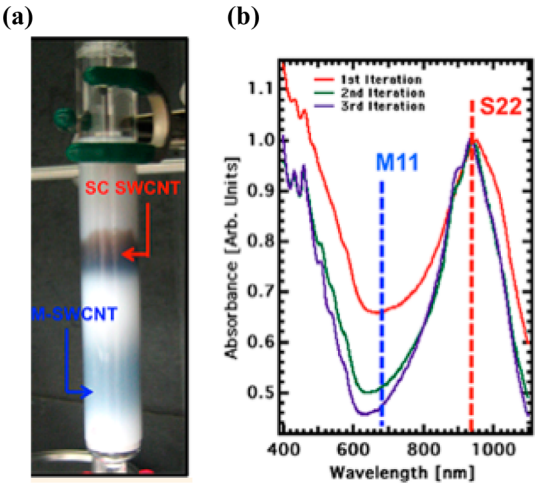


Figure 6. Sorting of CNTs *via* column chromatography. (a) Optical image of CNTs being sorted by electronic type *via* column chromatography. (b) UV−vis-NIR absorption spectra of sorted CNTs showing complete attenuation of the metallic region in the semiconducting (red curve) sample. Reproduced with permission from ref 31. Copyright 2013 American Chemical Society.

in an aqueous surfactant solution (typically sodium dodecyl sulfate). The solution is then loaded into a column containing a gel (typically Sephacryl). As the CNTs pass through the gel, the metallic and semiconducting CNTs move through the column at different rates (see Figure 6). It was found that the affinity of metallic and semiconducting CNTs are different, with metallic CNTs moving much faster through the column. The mechanism is likely that the metallic CNTs are more readily "shielded" from the column as the surfactants pack more densely around metallic CNTs than semiconducting (the polarizability of the metallic CNTs shield the charged head groups of the surfactant from each other).[35,36] High-purity semiconducting CNT solutions were prepared from this method with purities of 99.9%,[31] where the purity was verified electrically. In addition to simple electronic type sorting, single chirality sorting of small diameter CNTs was also shown.[34,36]

In addition to the surfactant-based separation methods, various types of polymer extractions are also very effective at sorting CNTs. Functionalized polythiophene compounds were shown to selectively wrap around semiconducting carbon nanotubes with high specificity.[37,38] This method is effective in sorting CNTs of various diameters and has shown purity levels of >99%. Polyfluorene derivatives were also shown to be extremely effective extracting semiconducting CNTs from organic solvents.[39−42] The process is extremely simple and scalable and merely involves sonicating the raw CNT powder in an organic solution of the polyfluorene deriviative followed by a simple centrifugation step. Impressive device results were achieved using these materials highlighting the high semiconducting purity.[43] Researches at NIST have recently demonstrated a polymer-extraction technique to sort both large and small diameter CNTs from solution.[44] This method relies on the sorting of CNTs between two immiscible aqueous phases that are formed by the addition of polymers. This method is especially simple and lends itself to iteration (up to 7 consecutive extractions were shown). The work follows a series of seminal papers from this same group that uses DNA to sort small-diameter CNTs by chirality.[45,46]

It is promising that several, somewhat disparate, techniques can be used to sort CNTs by electronic type. All of the techniques discussed here were used to produce >99% pure semiconducting CNT solutions. Although electrical characterization can be used to determine purity,[31,38,43] it will be difficult to make significant progress on the purity levels without the development of a high-throughput optical technique that can detect at least ppm levels of the metallic CNTs. In our view, the key bottleneck to achieving the purity levels necessary to implement the technologies is not only developing new sorting techniques, but also developing methods to accurately assess the purity at these high levels in solution.

CNT Placement. The development of a robust, scalable method to place CNTs on substrates with precision is one of the key challenges in the development of a competitive CNT logic technology. A competitive, high-performance CNT logic technology imposes several restrictions on the placement strategy. Perhaps most obvious is the requirement of high placement density with good alignment. As described in the previous section, high performance requires narrow devices, ∼50 nm, with 6−7 CNTs per channel (see Figure 3). Device variability has critical implications for placement *precision* and *uniformity*. That is, to reduce the variation in on-current, roughly the same number of CNTs must be placed in every device. As a practical matter, pitch variation must be less than about 5 nm. Finally, the placement strategy must be compatible with the purification strategy. Essentially all placement strategies can be divided into two different philosophical camps. In the first, pitch, alignment and purification are controlled *during the growth process*. The CNT array is usually grown on a special growth substrate, such as quartz, and is transferred to a CMOS-compatible substrate after growth. As described below, impressive strides have been made in the density and purification achievable during growth. The second approach envisions three completely separated process steps: *grow*, *purify*, *place*. CNTs are grown in bulk, separated in solution, and then placed from solution at precise locations on a CMOS-compatible substrate. Placement from solution is achieved by chemical self-assembly, or by external guiding using, *e.g.*, electric fields or capillary forces.

Aligned Growth. Aligned growth and transfer of CNTs has a long history. The first growth of CNTs *via* CVD was

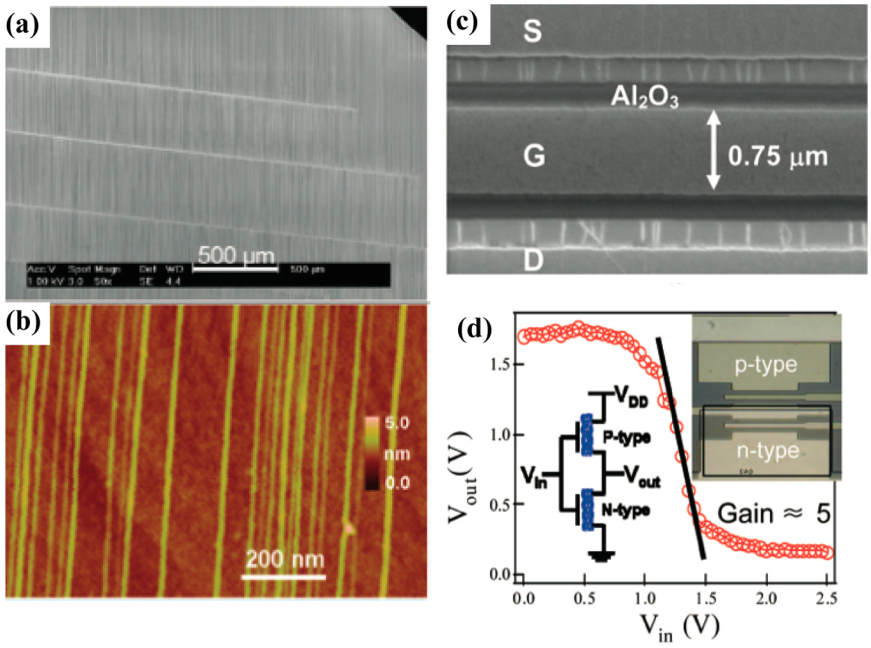


Figure 7. Aligned growth of CNTs. (a) Optical image of aligned CNTs grown on quartz and (b) a higher resolution AFM image. (c) SEM image of CNT-FETs fabricated from aligned CNTs and (d) electrical characteristics of an inverter fabricated with aligned CNTs. Reproduced with permission from ref 50 for panels a and b and ref 51 for panels c and d. Copyright 2008/2009 American Chemical Society.

carried out in 1996 by Dai *et al.* Later work by Kong *et al.* demonstrated CVD growth of CNTs at preselected areas of a patterned substrate.[47] These studies, and others, showed that very long (>10 μm), defect-free single-wall CNTs, in a useful diameter range (1−3 nm) could be grown parallel to the surface. One of the most important advances came in 2004 in the group of Joselevich. Ismach *et al.*[48,49] showed that special substrates could be used to induce alignment of the CNTs during growth. Specifically, they found that CNTs grew along the nanofacets (step bunches) that form on annealed miscut C-plane sapphire. In 2007, the Rogers group achieved essentially perfect alignment and good density (5 CNTs/μm) using flat ST cut quartz substrates.[49] They also demonstrated the transfer of the CNT array from the quartz to a CMOS-compatible substrate using a polyimide-coated gold film. Over the past few years, these methods have been improved to yield higher CNT density, with local values as high as 60 CNT/μm being recently reported (see Figure 7a,b).[50] Progress in growth and transfer has advanced to the point where wafer-scale CNT circuits can be reliably fabricated, although the device dimensions are still quite large (see Figure 7c,d).[51]

A reliable logic technology requires the elimination of metallic CNTs. In the growth-and-transfer scheme, this is done either during or after growth. Several approaches have been developed to make metallic CNTs insulating after growth. Perhaps the simplest approach is to "burn out" the metallic tubes after the devices are made. In each device, the gate is biased so that the semiconducting CNTs are off (*i.e.*, in a low conductance state). The current is increased until Joule heating destroys the metallic CNTs, at which point the device goes into the *off*-state. This approach was first demonstrated by Collins *et al.*,[52] and was used by Ryu *et al.*[51] in their wafer-scale circuit fabrication, as well as the fabrication of the first functional CNT computer.[8] A key drawback of this method is that large voltages are needed to drive sufficient current for burnout. Such large voltages would breakdown scaled dielectrics leaving the devices inoperable. In another impressive study, Zhang *et al.*[53] showed that metallic CNTs are selectively etched by exposure to a methane plasma at 400 C followed by annealing at 600 C. In the "medium" diameter range, 1.4−2.0 nm, essentially all metallic CNTs become insulating. For smaller diameters both species are etched, while for larger diameters neither is. The higher reactivity of metallic CNTs can also be exploited to selectively attack metallic CNTs. For example, An *et al.*[54] showed that by carefully controlling the concentration, diazonium reagents could be used to largely eliminate metallic CNTs while only a much smaller fraction of the semiconducting CNTs were affected. Remarkably, Ding *et al.*[55] showed that it is also possible to selectively eliminate metallic CNTs *during CVD growth* by the addition of methanol to the ethanol feed stock. The authors speculate that OH radicals from the methanol selectively etch metallic CNTs. From Raman spectroscopy, and transport measurements made on devices containing 500+ CNTs per device, it is inferred that the semiconducting fraction is about 95%. In a different approach, Jin *et al.*[56] showed that by flowing current through the metallic CNTs, the

heat generated will locally evaporate a thin-organic film (previously deposited over the CNT array) exposing just the metallic CNTs. A reactive ion etch then eliminates just the metallic CNTs, leaving behind a pristine array of semiconducting CNTs.

Collectively, these results suggest that aligned CVD growth may be capable of producing aligned CNTs with sufficient density and semiconducting purity for high-performance logic applications. There are several complex circuit demonstrations built on this platform,[57−59] including a functional nanotube computer[8] that further reinforces the utility of this approach. If this approach is to produce a scalable technology, the critical issue of pitch control must be addressed. Device variability is directly related to the pitch control. Even if the average CNT density is high, the number of CNTs per channel in a device will not be well controlled unless the CNT pitch is uniform. Variation in the number of CNTs leads to a variation in device on-current. Finally, it should be noted that the postgrowth purification methods noted above that remove metallic CNTs, or render them insulating, also adversely affect pitch control. Research groups from Stanford University are developing fault-tolerant design methodologies to address these issues with variability.[19]

CNT Placement from Solution. In contrast to directed growth, CNT placement from solutions proceeds by taking as-grown CNT powders, sorting the CNTs by electronic type and then placing them, from solution, into predefined locations on a substrate. The advantage over directed growth is that one can start with highly purified semiconducting CNTs and then place them onto a substrate with a specific pitch. Although the level of pitch control necessary for logic technology has not been demonstrated, remarkable progress was made toward that goal. The following sections will cover some of the recent progress in three broad strategies (a) directed chemical assembly using functionalized surfaces and/or functionalized CNTs, (b) directed assembly using electrostatic control, and (c) high density assembly of CNT films.

Directed Chemical Assembly. Early examples of CNT placement using self-assembly made use of surface modification by silane monolayers capable of interacting with the CNTs. An example of silanes capable of interacting with the CNT walls are aminosilanes.[60] To direct CNT placement on specific parts of the substrate, patterns of aminosilane monolayers on a surface were used. These patterns can be produced by (a) degradation of a methyl-terminated silane monolayer lithographically to generate patterned gaps not covered with a monolayer, and then filling the gaps left behind with an aminosilane monolayer;[61] (b) writing a pattern with e-beam lithography on a PMMA coating to generate patterned gaps not covered with a monolayer, and then filling the gaps left behind with an aminosilane monolayer;[62] (c) writing the pattern directly on the aminosilane monolayer with e-beam lithography.[63]

An alternative for the generation of nanopatterns capable of yielding high CNT placement selectivity was based on the selective wetting of monolayers that could be patterned directly using photolithography.[64,65] HfO_2 substrates were covered with a monolayer of a hydrophobic compound that could be transformed into a hydrophilic compound by exposure to UV light. This change in the chemical structure of the monolayer was used to generate surfaces with hydrophobic/hydrophilic patterns using standard photolithography and the patterning could be easily traced using AFM and SEM. These monolayers can be used for fast, selective CNT deposition over extremely large areas as shown in Figure 8a. Even though this approach has the advantage that no patterned oxides are needed for the self-assembly, the feature size demonstrated in this work was relatively large and

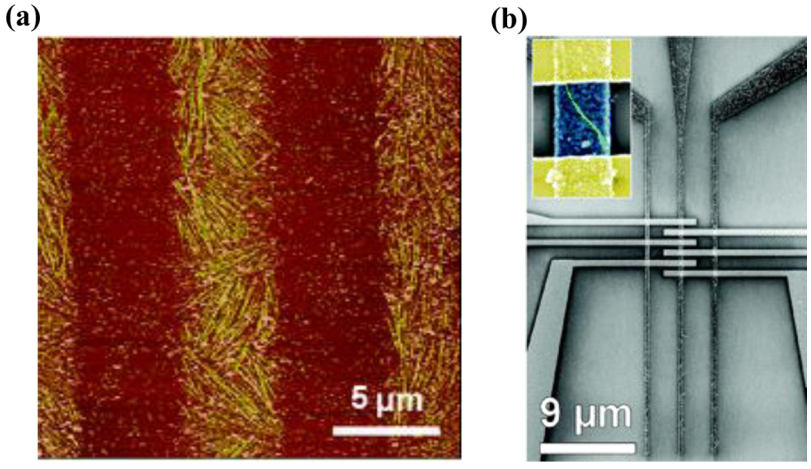


Figure 8. Directed assembly of CNTs. (a) AFM image of aligned CNTs fabricated by the directed assembly of CNTs onto a surface monolayer patterned by UV exposure (b) and SEM image of a series of CNT-FETs fabricated *via* the directed assembly of CNTs onto patterned substrates. Reproduced with permission from ref 64 for panel a and ref 67 for panel b. Copyright 2008/2006 American Chemical Society.

needs to be reduced in order to be usable for the fabricaton of arrays of individual CNT transistors.

Alignment of individual CNTs to obtain arrays of complex structures and shapes were demonstrated with substrates nanopatterned with dip-pen lithography.[66] Gold surfaces were modified with nanoscale patterns of a monolayer of a thiol-terminated compound with a carboxylic acid end group by using dip pen nanolithography and the rest of the surface was passivated with a monolayer of a methyl-terminated thiol. The modified surface is then exposed to CNTs dispersed in 1,2-dichlorobenzene, leaving CNTs assembled on the nanopatterns. Devices were not fabricated given the fact that the substrate was gold, which is not compatible with device fabrication, but this work demonstrated how complex assemblies of individual CNTs can be formed by selective modification and patterning of a given surface.

Another approach to promote selective interaction of individual CNTs with certain parts of the substrate is to covalently modify the CNTs. For instance, aryldiazonium salts bearing hydroxamic acid functionalities can be reacted with CNTs resulting in CNTs covalently functionalized, which as a result is decorated with hydroxamic acids.[67,68] The hydroxamic acid functionality on the CNT surface fosters CNT interaction with relatively basic metal oxides, which leads to highly selective deposition on Al_2O_3 or HfO_2 over SiO_2 as shown in Figure 8b. Individual CNT transistors can be obtained by deposition in narrow metal oxide trenches. Since the chemistry is reversible *via* heating, transistors obtained this way showed good *on*-currents and high *on*−*off* ratios of 10^7. Even though this is a technique feasible for transistor fabrication, the CNT density obtained this way was relatively low on large HfO_2 trenches with a width of 250 nm, and good densities need to be demonstrated using smaller trenches with a lower pitch.

The current state-of-the-art technique for high-density CNT placement from solution into narrow features is based on the directed assembly of negatively charged CNTs on positively charged monolayers.[69] CNTs dispersed in water with SDS as a surfactant are effectively negatively charged due to the sulfonate groups of SDS and substrates with patterned oxides of hafnium oxide and silicon dioxide can be coated with a positively charged self-assembled monolayer of 4-(*N*-hydroxycarboxamido)-1-methylpyridinium iodide (NMPI). When a solution of CNTs in water/SDS is used to cover the HfO_2/SiO_2 substrates, the formally negatively charged CNTs will be selectively placed on the positively charged parts of the substrate, which are areas of NMPI-coated HfO_2. This approach resulted in high-density deposition of up to 1×10^9 cm^{-2} CNTs with good CNT alignment over HfO_2 trenches of 70 nm with a 200 nm pitch. Single CNT transistors could be fabricated after CNT deposition and transistor performance were not affected by the chemicals used to mediate the CNT placement. This is a technique that affords thousands of CNT transistors at the same time and provides record density of placed CNTs. A further factor of 10 improvement in the placement density is necessary for use in a CNT logic technology.

Directed Assembly Using an Electric Field. Another method for the assembly and alignment of carbon nanotubes uses an electric fields (AC dielectrophoresis (DEP)) to align the CNTs between metal contacts. The advantages of this method are that it uses solutions of carbon nanotubes (so it is compatible with virtually all purification strategies), it can be used over large areas and allows for alignment and placement of CNTs at locations predefined by fabricated electrodes.

Chen *et al.*[70] shows an early demonstration of DEP assembly of single-walled CNTs. The CNTs were dispersed in ethanol, and the mixture was then exposed to a substrate with long, parallel gold electrodes. After application of an AC field across the electrodes, the CNTs are aligned across the electrode gap (along the direction of the AC field). The methodology has improved over the years to yield control over the density and orientation of the CNTs. In 2011, Shekhar *et al.*[71] demonstrated a CNT density of 30 CNT/μm, the highest reported to that date with any solution-based method (Figure 9a−c). The authors varied the CNT concentration in solution and the device channel lengths to gain fairly precise control over the CNT density.

In a 2007 paper by Vijayaraghavan *et al.*,[72] the authors demonstrate a large scale assembly of individual CNTs of several million devices per square centimeter using RF dielectrophoresis as shown in Figure 9d,e. Individual CNTs are aligned and placed between pairs of electrodes from solution. Additionally, under proper conditions, the process is self-limiting where, once a single CNT bridges the gap, no other CNTs are deposited in the same electrode pair. Fully functional CNTFETs were also fabricated showing that electrical contact is made between the CNT and the pair of electrodes.

Although electrodes used for the assembly can also be used as the source and drain contacts, this type of bottom contact is greatly inferior to contacts where the metal is deposited on the CNTs (bottom contact). To circumvent this limitation, Steiner *et al.*,[28] embedded the electrodes below a thin layer of hafnium oxide. The CNTs were then assembled *via* low-frequency DEP onto the gate dielectric at a density of 50 CNTs/μm. The contacts where then deposited last, onto the arrays of CNTs, thus producing a top contact. The resultant RF transistors had excellent transport properties and achieved an intrinsic current gain cutoff frequency of 153 GHz.

High-Density Solution-Based CNT Placement Techniques (LB/LS Assembly). Thin films of ordered organic and inorganic materials can be obtained by using

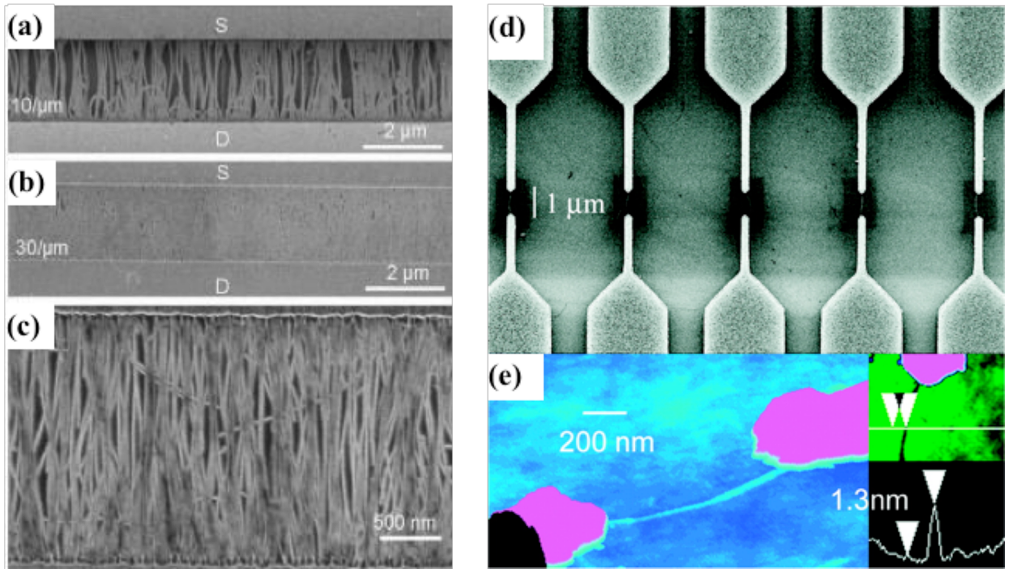


Figure 9. Scanning electron microscopy images of a DEP assembly with a density of (a) 10; (b) 20, and (c) 30 CNT/μm. (d) SEM image of individual CNT assembled between a series of source and drain electrodes by DEP and (e) AFM image of a single, aligned CNT. Reproduced with permission from ref 71 for panels a–c and ref 72 for panels d and e. Copyright 2011/2007 American Chemical Society.

Langmuir–Blodgett (LB) and Langmuir–Schaefer (LS) techniques. One approach to form a monolayer of single walled carbon nanotubes for LB/LS assembly is to disperse the CNTs in dichloroethane (DCE) by using poly(3p-phenylenevinylene-*co*-2,5-dioctyloxy-*m*-phenylenevinylene (PmPV), and then pour this organic solution onto a water phase.[73] Defect formation due to impurities or to the intrinsic polydispersity of CNTs can be avoided by using high purity SWCNTs. Very high density arrays of SWCNTs with very low defect occurrence were achieved by using purified solutions of SWCNTs, composed of 99% semiconducting CNTs.[31,74] The conjugated polymer (PmPV) could be removed by thermal annealing, and this technique was compatible with standard CMOS fabrication steps. Furthermore, reduction of the CNT pitch did not affect the electronic performance of devices fabricated by this method. This result is important not only for their implications in digital logic, but also for TFTs, sensors, batteries and flexible electronics. Even though the CNT densities of films prepared using LB/LS methods are among the highest reported and this technique is compatible with the use of purified, semiconducting CNTs, the main factor limiting the widespread application of this technique for digital logic based on individual CNT transistors is the lack of control of the CNT pitch.

Device-Level Challenges. *N-Type CNTFET.* Because CNTs are intrinsic semiconductors, all carriers must enter the channel by injection from the contacts, making the metal source/drain-to-CNT interface extremely important in CNTFET performance. For semiconductors that have dangling bonds at their surface, Fermi level pinning severely limits the effect of using metal contacts with different work functions to tune carrier injection. However, CNTs have no open bonds on their honeycomb carbon lattice and, hence, are not impacted by such pinning of the metal Fermi level to certain midbandgap states.[75] Without Fermi level pinning, the choice of metals with appropriate work functions is a valuable method for maximizing performance and even tuning polarity in CNTFETs.

With a work function of ~4.7 eV,[76,77] the Fermi level at midgap, no metal-induced gap states causing Fermi level pinning, and an average bandgap of 0.6 eV, CNTs naturally lend themselves to p-type FETs because of the ability of using a robust high work function metal for injecting holes into the valence band. It is often (mistakenly) assumed that CNTs are inherently p-type, which they are not. Rather, it is simply the fact that metals with high work function (such as Au or Pd) are used to make small SBH contacts to the valence band that has led to the majority of CNTFETs being p-type. To achieve electron injection to the conduction band for n-type devices requires either doping or low work function metal contacts.

Controlled doping CNTs is difficult. Substitutional or interstitial doping is not available. One feasible approach is to apply a layer of charged molecules to the CNT surface. This has been done in gas[78,79] or solution[80,81] phase, and with both n- and p-type dopants. While this charge-transfer doping approach has enabled some high performance CNTFETs, it is not without some challenges, including (1) low reproducibility/uniformity, (2) instability in air, (3) low compatibility with subsequent planarization of devices, and (4) sensitivity to high temperatures. Molecular dopants do not necessarily have all of these challenges, but they each have at least one of them to some degree.

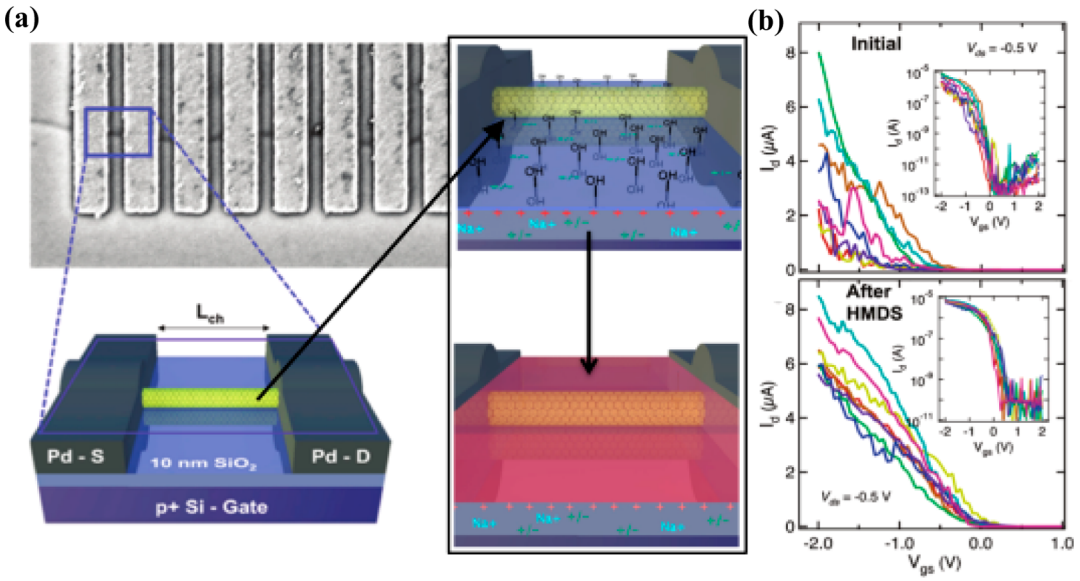


Figure 10. CNTFETs constructed along the same CNT showing large variation in threshold voltage. Gas-phase application of a hydrophobic monolayer passivates the hydroxylated surface and substantially lowers variation among the devices. Reproduced with permission from ref 88. Copyright 2012 American Chemical Society.

Another approach involves using low work-function metal oxides as the gate dielectric to effectively n-dope the CNT in the channel yielding n-type CNTFETs with excellent transport properties.[82]

There have been high performance n-type CNTFETs achieved by applying a layer of charged molecules to the spacer—or source/drain extension—regions (portions of the CNT channel between the gate and the source/drain) of a Pd-contacted device.[79] A further advantage of having such a CNTFET device with doped spacers is that the undesirable ambipolar conduction is largely suppressed because of the sizable barriers to carrier injection at the drain. It should also be noted that for the target technology node, the spacer thickness will be ~3 nm (lateral thickness) and no charge transfer was demonstrated at these layer thicknesses.

Establishing metal contacts with low barriers to electron injection is critical for n-type CNTFETs, even those with doped spacers (though in the case of doped spacers the Schottky barriers are thinned substantially by band movement from the doping). Perhaps the greatest challenge in working with low work function metals is their high propensity to oxidize, which among other things compromises their air stability and consistency of material quality. However, with appropriate passivation layers used to cap the metals, there have been demonstrations of n-type CNTFETs having superb performance, primarily using Y,[55] Sc,[83,84] or Er.[85] Such devices have exhibited near ideal performance for a single CNT—as good as p-type devices from Pd contacts. It has even been shown that under the appropriate metal deposition conditions, the yield of n-type CNTFETs can be increased to very near the level achievable by high work function metal p-type devices.[85] While more difficult to achieve than p-type CNTFETs, high performance n-type devices have seen considerable advancement in the past few years.

Hysteresis and V_t Variation. One highly promoted application space for CNTFETs is in chemical or biological sensing.[86,87] Because of their small size and extremely high specific surface area, the presence of virtually any adsorbate is readily detected by conductance transitions in a CNT. While excellent for sensing applications, the nanotube sensitivity to such stray charges is a challenge for high performance digital applications. This difficulty is manifest in the large variation of threshold voltage (V_t) among CNTFETs of the same geometry and the sizable hysteresis that is standard for most CNTFETs.[88]

Transfer curves from a set of CNTFETs built on the same nanotube are shown in Figure 10, where the threshold voltages span a range of ~0.8 V. The simple application of a hydrophobic self-assembled monolayer in vacuum to passivate (cover) the exposed CNT channel and surrounding dielectric surface is able to reduce the range of V_t by more than 50%. This reduction in V_t variation is a result of the vacuum deposition environment driving off stray charge adsorbates (*e.g.*, oxygen, water) and then passivating the hydroxylated surface to stave off any future adsorbates. Further, the hysteresis in the same devices was reduced on average from 500 to <50 mV over a gate-source bias (V_{gs}) range of 4 V at $V_{ds} = -0.5$ V. Such a dramatic reduction in variability is evidence that the variation is not intrinsic to the CNTs and is primarily a result of the channel being susceptible to stray charges in the vicinity. Either a technologically compatible passivation coating that can eliminate such charge or the ability to completely wrap a CNT in the gate is needed to address the variability problem.

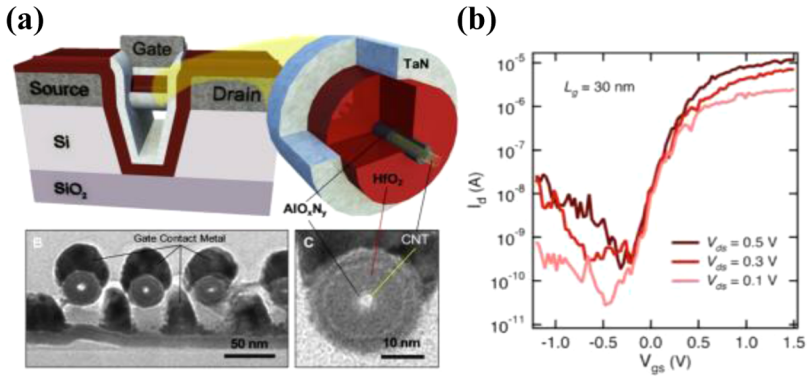


Figure 11. CNTFET with a gate-all-around (GAA) geometry. The transmission electron microscope images are cross sections of the GAA−CNT showing uniform coating of the gate stack on the nanotube. Subthreshold curves are from a 30 nm gate length *n*-type GAA−CNTFET. Reproduced with permission from ref 18. Copyright 2013 American Chemical Society.

Gate Dielectric and Structure. Because CNTs are made up of fully satisfied covalent carbon bonds, choosing a dielectric for CNTFETs is not related to Fermi level pinning or passivating surface states, as is the case for most other semiconductors and the plague for III−V materials,[89] but rather what dielectric can be scalable with a compatible deposition process for the CNT. The most common fabrication method for depositing high quality high-κ dielectrics is atomic layer deposition (ALD), which is a chemical vapor deposition process that relies on gaseous precursors to react with surface states to form a dielectric one layer at a time.[90] Having no surface states, CNTs are not naturally compatible with ALD. To overcome this limitation, either bottom-gate CNTFETs were used,[91,92] adhesion layers were applied to enable ALD nucleation on CNTs,[93,94] or metal films (*i.e.*, Yttrium) is deposited and then subsequently oxidized.[95]

For bottom-gated devices, the dielectric is completely formed prior to placing the nanotubes on the substrate, making it a great option as far as dielectric choice, scalability, and quality are concerned. But the bottom gate geometry can also be tricky for manufacturability, so it is desirable to have other options. Adhesion layers for ALD nucleation have been demonstrated in the form of DNA molecules that wrap CNTs[96] or gas-phase functional layers formed in a CVD chamber prior to ALD.[93] The latter approach is more favorable in that it employs highly compatible oxide layers that will not compromise the needed low equivalent oxide thickness (EOT) of the final device structure. Once the adhesion layer is in place, ALD can be used to deposit the high-κ material of choice.

Because CNTs are not substrate-bound, there is a lot of freedom in designing the gate structure. CNTFETs are typically fashioned with either bottom- or top-gate geometries. While the top-gate does provide an omega-shaped gate structure, the electrostatics are not appreciably different from the bottom-gate, cylinder-on-plate structure. Top gates more closely mimic the structure of Si MOSFETs but have been challenging to realize with the inability to use reactive ion etching (RIE) in the presence of CNTs (nanotubes are readily etched away in a reactive ion environment). Regardless of the gate geometry, the gate metal work function provides a 1:1 control over the device threshold voltage to enable the tuning of V_t in a final architecture.[59]

The ultimate gate structure for CNTFETs is one that completely wraps the nanotube channel in a gate-all-around (GAA) fashion.[94,97] GAA is so natural for CNTs that it has been used for virtually all simulation studies of CNTFETs.[98−100] A recent demonstration of GAA−CNTFETs is highlighted in Figure 11.[18] Although the GAA provides the ideal electrostatic structure for nanotubes, it is a mistake to conclude that this marginal improvement in electrostatics is critical for achieving CNTFETs with sub-10 nm channels. The ultrathinness of a nanotube (<2 nm) enables excellent gate control of the channel even with only a bottom gate.[10] Actually, the primary motivation for GAA is that the gate encompasses the CNT, shielding it from stray charge, screening interactions, or other local variations. As pointed out previously, nanotubes are sensitive to any charge in their vicinity, and the GAA is the only complete solution for addressing this challenge.

Contact Scaling. It is instinctual to focus on channel length (L_{ch}) when discussing the scaling of any type of FET because short channel effects are known to be a result of small L_{ch}. However, for an FET to be densely integrated in a useful digital technology, the length of the contacts (source and drain) must be scaled as aggressively as the channel. An illustration of these two lengths in a CNTFET is given in Figure 12. The fact that there has been less focus on contact length (L_c) scaling for nanoelectronic devices is not because it has not been a challenge for Si MOSFETs: small contact lengths have led to dramatic increases in series resistance, which compromises *on*-state performance. It is most probable that the lack of attention to L_c in nanomaterial-driven FETs is simply because (1) short channel effects from L_{ch} scaling is a bigger concern for Si MOSFETs and thus more popular to address and (2)

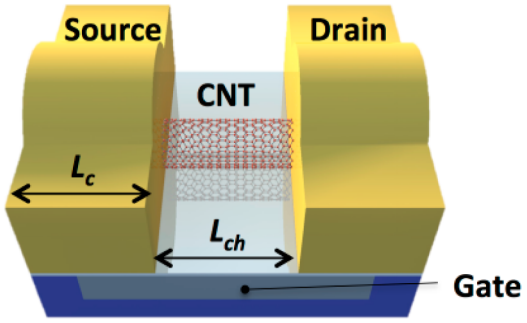


Figure 12. Schematic of a CNTFET with the contact length (L_c) and channel length (L_{ch}) identified.

there is less motivation to consider L_c when there are still short channel effects present.

For CNTFETs, the first study to consider the impact of contact scaling revealed an important challenge for realizing high performance, ultrasmall devices: contact resistance (R_c) exhibits an inverse dependence on L_c, similar to MOSFETs.[9,101] While some previous studies had explored this trend for large multiwalled carbon nanotubes,[102] this R_c *vs* L_c dependence in CNTFETs clearly defined the balance between L_{ch} and L_c scaling in these devices for achieving optimal performance.

The reason for R_c showing strong dependence on L_c is different than for MOSFETs. A metal–CNT contact is a 3D–1D, metal–semiconductor interface, creating a very different scenario from the standard 3D–3D, silicide–semiconductor interface. Some had even projected short contacts to improve metal–CNT R_c by maximizing the electric field at the interface.[103,104] There have been theoretical studies that try and make sense of the observed scaling behavior, but they all deal with carrier injection between the metal–CNT and have not found a way of considering how transport in the metal-covered CNT contributes to R_c.[101,105–107] Very recent results exploring different contact metals has revealed that the lowest contact resistance at small L_c will not necessarily come from the metal that yields the lowest resistance at long lengths.[108] There are a myriad of possibilities for improving the L_c scaling behavior for CNTFETs that should come to light in the ensuing years, including the exploration of other contact metals and modified metal–CNT interfaces.

OUTLOOK

Recent experimental results, coupled with system level modeling, show that carbon nanotube transistors have the intrinsic properties that enable them to be a major disruptive force in the electronics industry. Despite their remarkable intrinsic properties, several materials and device-related challenges remain unresolved and impede the implementation of the material. In our view, the most important, unresolved problems include (1) how do we quantify the purity of semiconducting carbon nanotubes at purity levels above 99.9%, (2) how do we obtain wafer scale assembly and alignment of CNTs with a narrow and controlled pitch (either through aligned growth or directed assembly), and (3) how do we build devices with scaled contacts (<12 nm) without introducing unacceptable levels of contact resistance. The difficulty in continued scaling in traditional CMOS has created an opportunity for the current community of engineers, chemists and materials scientists to transform the industry. It is our view that no entity can solve the remaining challenges alone, but that a sustained effort across industry and academia is the only path to fulfilling the promise of these emerging materials.

Conflict of Interest: The authors declare no competing financial interest.

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